Docket No. 55561 (70820)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Y. Kubota et al.	CONF. NO.:	7275
U.S. SERIAL NO.:	09/775,167	EXAMINER:	S. Kumar
FILED:	February 1, 2001	GROUP:	2629

FOR: SHIFT REGISTER CIRCUIT CAPABLE OF REDUCING CONSUMPTION OF POWER WITH REDUCED CAPACITIVE LOAD OF CLOCK SIGNAL LINE AND IMAGE DISPLAY DEVICE INCLUDING IT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO OFFICE ACTION

Applicants are in receipt of the Office Action dated April 2, 2007 of the above-referenced application. Applicants respond to the Office Action as follows.

Claims 1-25 are pending in the application.

Claims 1-5, 14, and 25 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,289,518 to Nakao in view of "Applicant's Admitted Prior Art (AAPA)." The remaining claims were rejected over prior art including the Nakao reference and AAPA. These rejections are respectfully traversed.

The proposed combination of Nakao in view of AAPA does not teach or suggest a shift register circuit in which an input control signal of a transfer gate of a corresponding register block is brought into an ON-state only in a specified period when an output of the corresponding flip-flop **changes**.

On page 2, last paragraph of the Office Action of 04/02/2007, it was admitted that the Nakao reference does not teach or suggest "the input control signal of the transfer gate being brought into an ON-state [only] when the output of the flip-flop … changes."

AAPA was cited for allegedly teaching "this feature in Figs. 41A-J, and pages 6-8 of the specification, where ctl1 corresponds to out1, ctl2 corresponds to out2, etc." (page 3, lines 1-2 of the Office Action of 04/02/2007).

As shown in PRIOR ART FIGS. 41A-41J, the control signal CTL1 is brought into an ON-state during the entire period in which the output OUT1 of the flip-flop is **active**, which includes not only the time in which the output of the flip-flop "changes," but also the remaining time in which the output OUT1 is active.

As described in the Background section of the specification, according to the operating circuit depicted in FIGS. 41A-41J, "a plurality of nodes in the shift register circuit become concurrently active when the scanning pulse width of the shift register circuit is long," which results in a plurality of level shift circuits being brought into an operating state, thus increasing the consumption of power (see specification at page 8, line 16 to page 9, line 5). Therefore, the Applicants' claimed invention offers advantages over the conventional operating circuit illustrated in FIGS. 41A-41J.

Even if AAPA was somehow combined with the Nakao reference, the proposed combination would not teach or suggest a shift register circuit in which an input control signal of a transfer gate of a corresponding register block is brought into an ON-state only in a specified period when an output of the corresponding flip-flop **changes**.

Instead, AAPA teaches that a control signal is brought into an ON-state during the entire period in which the output OUT1 of the flip-flop is **active**, and thus is not limited to the time period in which the output of the flip-flop **changes**, as required in independent claims 1 and 25.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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